Papers in the following areas are solicited

- Advanced SOI materials and structures. Physical mechanisms and innovative SOI-like devices.
- New channel materials for CMOS: strained Si, strained SOI, SiGe, GeOI, III-V and high mobility materials on insulator; carbon nanotubes; graphene and other two-dimensional materials.
- Properties of ultra-thin films and buried oxides, defects, interface quality. Thin gate dielectrics: high-κ materials for switches and memory.
- Nanometer scale devices: technology, characterization techniques and evaluation metrics for high performance, low power, reliability, high frequency and memory applications.
- Alternative transistor architectures including FD SOI, Nanowire, FinFET, MuGFET, vertical MOSFET, FeFET and Tunnel FET, MEMS/NEMS, Beyond-CMOS nanoelectronic devices.
- New functionalities in silicon-compatible nanostructures and innovative devices representing the More than Moore domain, nanoelectronic sensors, biosensor devices, energy harvesting devices, RF devices, imagers, etc.
- CMOS scaling perspectives; device/circuit level performance evaluation; switches and memory scaling. Three-dimensional integration of devices and circuits, heterogeneous integration.
- Transport phenomena, compact modeling, device simulation, front- and back-end process simulation.
- Advanced test structures and characterization techniques, parameter extraction, reliability and variability assessment techniques for new materials and novel devices.

Invited Speakers

Dr. Ionut RADU, SOITEC: "SOI technology: from niche to mainstream applications"
Dr. Anabela VELOSO, IMEC: "Nanowire for Ultra-Scaled, High-Density Logic and Memory Applications"
Dr. Marc GAILLARDIN, CEA: "Radiation effects in innovative devices"
Prof. Ru HUANG, Peking University: "Steep slope devices"