EUROSOI – ULIS 2019 – 1st CALL FOR PAPER

April 1 – 3, 2019 – Grenoble, France

Abstract submission deadline : January 15, 2019

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The template for the 2-page abstract is available at the conference website:

https://eurosoiulis2019.sciencesconf.org

The fifth joint EUROSOI-ULIS conference will be hosted by Grenoble Institute of Technology and CEA-LETI in Grenoble. The organizing committee invites scientists and engineers working on SOI technology and advanced nanoscale devices to actively participate by submitting high quality, original contributions.

The authors of the accepted contributions will be requested to provide a 4-page extended abstract which will be included in the conference proceedings (with IEEE technical sponsorship and ISBN index) and in the IEEE Xplore® digital library. Outstanding papers will be invited for publication in a special issue of Solid-State Electronics. A best paper award will be attributed by the SINANO institute. The conference will be followed on April 4th by satellite events.

Papers in the following areas are solicited

- Advanced SOI materials and structures. Physical mechanisms and innovative SOI-like devices.
- New channel materials for CMOS: strained Si, strained SOI, SiGe, GeOI, III-V and high mobility materials on insulator; carbon nanotubes; graphene and other two-dimensional materials.
- Properties of ultra-thin films and buried oxides, defects, interface quality. Thin gate dielectrics: high-κ materials for switches and memory.
- Nanometer scale devices: technology, characterization techniques and evaluation metrics for high performance, low power, reliability, high frequency and memory applications.
- Alternative transistor architectures including FDSOI, Nanowire, FinFET, MuGFET, vertical MOSFET, FeFET and Tunnel FET, MEMS/NEMS, Beyond-CMOS nanoelectronic devices.
- New functionalities in silicon-compatible nanostructures and innovative devices representing the More than Moore domain, nanoelectronic sensors, biosensor devices, energy harvesting devices, RF devices, imagers, etc.
- CMOS scaling perspectives; device/circuit level performance evaluation; switches and memory scaling. Three-dimensional integration of devices and circuits, heterogeneous integration.
- Transport phenomena, compact modeling, device simulation, front- and back-end process simulation.
- Advanced test structures and characterization techniques, parameter extraction, reliability and variability assessment techniques for new materials and novel devices.